CONTINUOUS INTERLEAVE BURST ACCESS

Cross-Reference to Related Application(s)

This application is a continuation of U.S. Patent Application No. 10/118,299, filed on April 8, 2002, which is a continuation of U.S. Patent Application No. 08/675,139, filed on July 3, 1996, now U.S. Patent 6,401,186 issued on June 4, 2002, which are hereby incorporated by reference.

Technical Field of the Invention

The present invention relates generally to memory devices and in particular the present invention relates to burst access memory devices.

Background of the Invention

There is a demand for faster, higher density, random access memory integrated circuits which provide a strategy for integration into today's personal computer systems. In an effort to meet this demand, numerous alternatives to the standard DRAM architecture have been proposed. One method of providing a longer period of time when data is valid at the outputs of a DRAM without increasing the fast page mode cycle time is called Extended Data Out (EDO) mode. In an EDO DRAM the data lines are not tri-stated between read cycles. Instead, data is held valid after CAS* goes high until sometime after the next CAS* low pulse occurs, or until RAS* or the output enable (OE*) goes high. Determining when valid data will arrive at the outputs of a fast page mode or EDO DRAM can be a complex function of when the column address inputs are valid, when CAS* falls, the state of OE* and when CAS* rose in the previous cycle. The period during which data is valid with respect to the control line signals (especially CAS*) is determined by the specific implementation of the EDO mode, as adopted by the various DRAM manufacturers.

Yet another type of memory device is a burst EDO memory which adds the ability to address one column of a memory array and then automatically address additional columns in a pre-determined manner without providing the additional column addresses on external address lines. These memory devices use a column access input to access the memory array columns.

A latency is experienced during a read operation. That is, output data is not immediately available following an externally applied column address. The latency is required to prepare, access and sense data stored at the new address.

Regardless of the type of memory, a processor receiving data from a memory may delay a new memory read operation until a prior read is complete. This delay results in a delay of new valid data. For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a memory system which anticipates the address of a new memory read operation to reduce or eliminate delays in valid data.

Summary of the Invention

The above mentioned problems with accessing data stored in a memory device and other problems are addressed by the present invention and which will be understood by reading and studying the following specification. A system is described which anticipates the memory address to be used in future data read operations as requested by a microprocessor.

In particular, the present invention describes a system comprising a synchronous memory device having addressable memory cells, a microprocessor coupled to the synchronous memory device for data communication with the addressable memory cells, the microprocessor further initiating a data read operation at a first memory cell address. A memory controller is connected to the microprocessor and the synchronous

memory device. The memory controller produces a second memory cell address and initiates a read operation in anticipation of a second data read operation at a new memory cell address provided from the microprocessor.

Alternatively, a system is described which comprises a microprocessor, a burst access memory having addressable memory cells for providing data in response to a read request from the microprocessor, the read request including a start memory cell address, and address generation circuitry included in the burst access memory for generating a memory cell address and initiating a read operation in anticipation of a read request from the microprocessor.

In still another embodiment, a method of continuously outputting data from a synchronous memory device is described. The method comprises the steps of providing a read request from a microprocessor, the read request including a memory cell start address for the synchronous memory device. The method further including the steps of initiating a read operation using a memory controller in response to the read request, and outputting data from the synchronous memory device in response to the memory controller. A new memory address is generated in anticipation of a second read request from the microprocessor, the second read request including a second memory cell start address. Finally, a second read operation is initiated and data is output from the synchronous memory device starting at the new memory address.

Brief Description of the Drawings

Figure 1 is a burst access memory device;

Figure 2 is a table which shows linear and interleaved addressing sequences;

Figure 3 is a timing diagram for performing a burst read followed by a burst write of the device of Figure 1;

Figure 4 is a timing diagram depicting burst write access cycles followed by burst read cycles of the device of Figure 1;

Figure 5 illustrates a typical system of the present invention;

Figure 6 is a timing diagram of successive read operations of a burst access memory;

Figure 7 is a timing diagram of successive read operations of the system of Figure 5;

Figure 8 is a timing diagram of an operation of an SDRAM used in the system of Figure 5; and

Figure 9 is a timing diagram of another operation of the SDRAM of Figure 8.

Detailed Description of the Invention

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the inventions may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present inventions. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present inventions is defined only by the appended claims.

Figure 1 is a schematic representation of a sixteen megabit device 84 designed to operate in a burst access mode. The device is organized as a 2 Meg x 8 burst EDO DRAM having an eight bit data input/output path 10 providing data storage for 2,097,152 bytes of information in the memory array 12. An active-low row address strobe (RAS*) signal 14 is used to latch a first portion of a multiplexed memory address, from address inputs AO through A10 16, in latch 18. The latched row address 20 is decoded in row decoder 22. The decoded row address is used to select a row of the memory array 12. An active-low column address strobe (CAS*) signal 24 is used to

latch a second portion of a memory address from address inputs 16 into column address counter 26. The latched column address 28 is decoded in column address decoder 30. The decoded column address is used to select a column of the memory array 12.

In a burst read cycle, data within the memory array located at the row and column address selected by the row and column address decoders is read out of the memory array and sent along data path 32 to output latches 34. Data 10 driven from the burst EDO DRAM may be latched external to the device in synchronization with a clock signal after a predetermined number of clock cycle delays (latency). For a two cycle latency design, the first CAS* falling edge is used to latch the initial address for the burst access. The first burst data from the memory is driven from the memory after the second CAS* falling edge, and remains valid through the third CAS* falling edge. Once the memory device begins to output data in a burst read cycle, the output drivers 34 will continue to drive the data lines without tri-stating the data outputs during CAS* high intervals dependent on the state of the output enable and write enable (OE* and WE*) control lines, thus allowing additional time for the system to latch the output data. Once a row and a column address are selected, additional transitions of the CAS* signal are used to advance the column address within the column address counter in a predetermined sequence. The time at which data will be valid at the outputs of the burst EDO DRAM is dependent only on the timing of the CAS* signal provided that OE* is maintained low, and WE* remains high.

The address may be advanced linearly, or in an interleaved fashion for maximum compatibility with the overall system requirements. Figure 2 is a table which shows linear and interleaved addressing sequences for burst lengths of 2, 4 and 8 cycles. The "V" for starting addresses Al and A2 in the table represent address values that remain unaltered through the burst sequence. The column address may be advanced with each CAS* transition, or each pulse. When the address is advanced with each transition of the CAS* signal, data is also driven from the part after each transition following the

device latency which is then referenced to each edge of the CAS* signal. This allows for a burst access cycle where the CAS* toggles only once (high to low or low to high) for each memory cycle.

In the burst access memory device, each new column address from the column address counter is decoded and is used to access additional data within the memory array without the requirement of additional column addresses being specified on the address inputs 16. This burst sequence of data will continue for each CAS* falling edge until a predetermined number of data accesses equal to the burst length has occurred. A CAS* falling edge received after the last burst address has been generated will latch another column address from the address inputs 16 if CAS* is low and a new burst sequence will begin. Read data is latched and output with each falling edge of CAS* after the first CAS* latency. For a burst write cycle, data 10 is latched in input data latches 34. Data targeted at the first address specified by the row and column addresses is latched with the CAS* signal when the first column address is latched (write cycle data latency is zero). Other write cycle data latency values are possible; however, for today's memory systems, zero is preferred. Additional input data words for storage at incremented column address locations are latched by CAS* on successive CAS* pulses. Input data from the input latches 34 is passed along data path 32 to the memory array where it is stored at the location selected by the row and column address decoders. As in the burst read cycle previously described, a predetermined number of burst access writes will occur without the requirement of additional column addresses being provided on the address lines 16. After the predetermined number of burst writes has occurred, a subsequent CAS* will latch a new beginning column address, and another burst read or write access will begin.

The write enable signal is used in burst access cycles to select read or write burst accesses when the initial column address for a burst cycle is latched by CAS*. WE* low at the column address latch time selects a burst write access. WE* high at the

column address latch time selects a burst read access. A low to high transition within a burst write access will terminate the burst access, preventing further writes from occurring. A high to low transition on WE* within a burst read access will likewise terminate the burst read access and will place the data output 10 in a high impedance state. Transitions of the WE* signal may be locked out during critical timing periods within an access cycle in order to reduce the possibility of triggering a false write cycle. After the critical timing period, the state of WE* will determine whether a burst access continues, is initiated, or is terminated. Termination of a burst access resets the burst length counter and places the DRAM in a state to receive another burst access command. Both RAS* and CAS* going high during a burst access will also terminate the burst access cycle placing the data drivers in a high impedance output state, and resetting the burst length counter. The burst length counter is preferably included in the control logic circuit 38. The burst length counter is used to keep track of how many cycles are performed in a burst access, and is not the same as the address counter which generates the burst addresses for the memory array.

A minimum write enable pulse width is only required when it is desired to terminate a burst read and then begin another burst read, or terminate a burst write prior to performing another burst write with a minimum delay between burst accesses. In the case of burst reads, WE* will transition from high to low to terminate a first burst read, and then WE* will transition back high prior to the next falling edge of CAS* in order to specify a new burst read cycle. For burst writes, WE* would transition high to terminate a current burst write access, then back low prior to the next falling edge of CAS* to initiate another burst write access.

A basic implementation of the device of Figure 1 may include a fixed burst length of 4, a fixed CAS* latency of 2 and a fixed interleaved sequence of burst addresses.

The burst access memory has been described with reference to several embodiments. Just as fast page mode DRAMs and EDO DRAMs are available in numerous configurations including x1, x4, x8 and x16 data widths, and 1 Megabit, 4 Megabit, 16 Megabit and 64 Megabit densities; the burst access memory device may take the form of many different memory organizations.

Figure 3 is a timing diagram for performing a burst read followed by a burst write of the device of Figure 1. In Figure 3, a row address is latched by the RAS* signal. WE* would be low when RAS* falls for an embodiment of the design where the state of the WE* pin is used to specify a burst access cycle at RAS* time. Next, CAS* is driven low with WE* high to initiate a burst read access, and the column address is latched. The data out signals (DQ's) are not driven in the first CAS* cycle. On the second falling edge of the CAS* signal, the internal address generation circuitry advances the column address and begins another access of the array, and the first data out is driven from the device after a CAS* to data access time (tCAC). Additional burst access cycles continue, for a device with a specified burst length of four, until the fifth falling edge of CAS* which latches a new column address for a new burst read access. WE* falling in the fifth CAS* cycle terminates the burst access, and initializes the device for additional burst accesses. The sixth falling edge of CAS* with WE* low is used to latch a new burst address, latch input data and begin a burst write access of the device. Additional data values are latched on successive CAS* falling edges until RAS* rises to terminate the burst access.

Figure 4 is a timing diagram depicting burst write access cycles followed by burst read cycles. As in Figure 3, the RAS* signal is used to latch the row address. The first CAS* falling edge in combination with WE* low begins a burst write access with the first data being latched. Additional data values are latched with successive CAS* falling edges, and the memory address is advanced internal to the device in either an interleaved or sequential manner. On the fifth CAS* falling edge a new column address

and associated write data are latched. The burst write access cycles continue until the WE* signal goes high in the sixth- CAS* cycle. The transition of the WE* signal terminates the burst write access. The seventh CAS* low transition latches a new column address and begins a burst read access (WE* is high). The burst read continues until RAS* rises terminating the burst cycles.

Continuous Burst Access

Figure 5 illustrates a typical system application of the burst access memory described above. A microprocessor 80 and memory controller 82 are connected to the memory device 84. Memory device 84 may be any type of module, for example a single in-line memory module (SIMM), dual in-line memory module (DIMM), or a multi-chip module (MCM). The microprocessor communicates data with the memory device and provides instructions to the memory controller. It will be appreciated by those skilled in the art that a system using a burst memory may have to wait up to four CAS* cycles to read additional data from the memory. This delay is due to both latency and buffering. For example, in a four word burst access, two to four extra CAS* pulses may be required from the memory controller to communicate the last burst data to the microprocessor.

If the data from a memory burst read is needed by the microprocessor to determine a new memory address, unnecessary delay may be experienced. That is, the time needed to initiate a new read operation after the termination of a prior read is avoidable delay. For comparison, Figure 6 illustrates successive read operations of a burst access memory where the second read operation is not initiated until after the first read operation is complete. The burst access illustrated has a latency of three CAS* cycles. The data, therefore, is output from the memory starting on the third CAS* falling edge. A three cycle delay in output data is incurred following the end of the COLm data sequence and the beginning of the COLn data sequence.

The present invention includes memory controller 82 which initiates a read operation at a memory address determined to be the most likely next address to be requested by the microprocessor 80. The memory controller, therefore, anticipates the next address to be requested by the microprocessor. If the microprocessor requests data from the memory which corresponds to the new address determined by the memory controller, access time is saved. If the new memory address requested by the microprocessor is different from that determined by the memory controller, no additional access time is incurred by the system than would be required from a system not incorporating the present invention. The memory controller can include an address comparator which compares an address requested by the microprocessor and a new address generated by the memory controller. If the addresses are the same, the memory controller continues with the new burst read operation. If the address requested by the microprocessor is different from that produced by the memory controller, a new read operation is initiated at the address provided by the microprocessor. Alternatively, the microprocessor can be programmed such that the next address generated by the memory controller is known. This embodiment allows the microprocessor to use the new data without requesting a read operation. The burst memory 84 can include an address generation circuit which determines the next address to be requested by the microprocessor. The memory controller, therefore, does not determine the next address.

Continuous Read Operation

Figure 7 is a timing diagram of a portion of a continuous burst read operation in accordance with a preferred embodiment of the present invention. A first column address (COLm) identified by the microprocessor 80 is provided to the memory 84. The first address is used as the starting address for the burst read operation. The internal address is advanced in either a sequential or interleaved manner as described above with reference to Figure 2. The burst access illustrated has a latency of three CAS* cycles.

The data is burst read from the memory starting on the third CAS* falling edge. A new column address (COLn) is provided on the address lines by the memory controller 82 on the fifth CAS* cycle. A data sequence originating at the new column address is burst out starting on the seventh CAS*, incurring no data output delay. The microprocessor 80 can request data from the memory controller between the fifth and eighth CAS* cycle without incurring a delay. If the microprocessor requests data from an address different than the address generated by the memory controller, data provided on the DQ lines is ignored by the microprocessor until the microprocessor's new address is accessed. A latency delay will be experienced similar to that shown in Figure 6.

It will be appreciated by those skilled in the art, that the present invention can include an address generator internal to the memory control circuitry 38 which produces a new column address if a valid new address is not provided on the external address lines. To assist the memory controller, the output enable (OE*) input can be used to indicate the presence of a valid address on the address lines. Further, additional counter circuitry can be added to the memory to enable the memory to output a full length column sequence.

The column address generated in the absence of a request by the microprocessor can be determined in any number of ways. The new address can be produced by repeating the prior sequence with an advanced most significant bit, as shown in Tables 1 where X represents address most significant bits (MSB's) followed by bits A1 and A0. In Table 1 an interleaved address sequence is shown for a burst length of 4. The next burst sequence start address is derived by incrementing the MSB's (X) and by repeating the initial LSB's (A1, A0). In Table 2 the next burst sequence start address is derived by incrementing the MSB's and resetting the LSB's to 0, 0. Either of these methods may be utilized for other burst length options, and for other addressing sequences.

START ADDRESS	NEXT ADDRESS
X 0 1	(X+1) 0 1
X 0 0	(X+1) 0 0
X 1 1	(X+1) 1 1
X 1 0	(X+1) 1 0

TABLE 1

START ADDRESS	NEXT ADDRESS
X 0 1	(X+1) 0 0
X 0 0	(X+1) 0 1
X 1 1	(X+1) 1 0
X 1 0	(X+1) 1 1

TABLE 2

An alternate method of bursting data in the absence of a request by the microprocessor is a full page burst access. That is, the memory outputs data from the full memory page starting at the address next column address.

Figure 8 illustrates one operation of the system of an SDRAM which can be used in the system of Figure 5. For a detailed description of a SDRAM see 1995 DATA SHEET 16M DRAM, provided by Samsung Electronics and incorporated herein by reference. At time t1, the microprocessor 80 issues a read command for column X. At time t2 controller 82 issues a read command to the memory 84 for column X. The memory in this illustration has a latency of 3 and burst length of 4. Data from column X is valid from time t5 to t8. At time t6, the memory controller issues an anticipatory read

command for column address Y. At time t8 the microprocessor issues a read command for column address Y. Valid data from column Y is provided from time t9 to t12.

Referring to Figure 9, at time t1, the microprocessor 80 issues a read command for column X. At time t2 controller 82 issues a read command to the memory 84 for column X. The memory in this illustration has a latency of 3 and burst length of 4. Data from column X is valid from time t5 to t8. At time t6, the memory controller issues an anticipatory read command for column address Y. At time t8 the microprocessor issues a read command for column address Z. Valid data from column Y is provided from time t9 to t11. Valid data from column Z is provided starting at time t12.

It will be appreciated that in the operation of Figure 8 three clock cycles are saved by correct anticipation of the next read address. In the operation illustrated in Figure 9, the data from column Y is ignored while the microprocessor waits for data from column Z.

CONCLUSION

A system has been described which uses a burst access memory and a memory controller to anticipate the memory address to be used in future data read operations as requested by a microprocessor. Either the memory controller or the memory device initiates a burst read operation starting at a memory address generated thereby. The microprocessor can, therefore, wait to initiate a data read without suffering a time delay. The new address is generated in a predetermined pattern. The memory controller can include a comparator to compare an address provided by the microprocessor with the predetermined address. The memory controller can thereby ignore a read request from the microprocessor which corresponds to the generated address. Alternately, the microprocessor can withhold a request if the correct address has been initiated by the memory controller.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. For example, synchronous DRAMs can be used in place of the burst access memory device without departing from the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.